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ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/853,226	STRONGIN, GEOFFREY S.
	Examiner	Art Unit	
	Kevin P. Rizzuto	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2005*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,35,41,42 and 53* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,35,41,42 and 53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date ___.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15, 35, 41-42 and 53 have been examined.

2. Acknowledgement of papers filed: Amendment filed on 12/16/2005. The papers

filed have been placed on record.

Apparatus Claims -- Functional Language

3. Examiner notes that multiple instances of functional language are present in the

apparatus claims. A claimed apparatus must differ in structure from prior art

references; therefore, functional limitations are not to be read into the claims. See

"MPEP 2114 [R-1] Apparatus and Article Claims — Functional Language".

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or
> described as set forth in section 102 of this title, if the differences between the subject
> matter sought to be patented and the prior art are such that the subject matter as a whole
> would have been obvious at the time the invention was made to a person having ordinary
> skill in the art to which said subject matter pertains. Patentability shall not be negatived
> by the manner in which the invention was made.

5. **Claims 1, 2 and 5-15 are rejected under 35 U.S.C. 103(a) as being**

unpatentable over Gafken et al., U.S. Patent 5,826,007, herein referred to as

Gafken, in view of Yishay et al., U.S. Patent 5,704,039, herein referred to as

Yishay.

6. As per claim 1, Gafken teaches a processor, comprising:

-A first register configured to store one or more enable bits for a hardware debugging mode: (Column 8, lines 21-44, figure 7, R/L register, if the R/L register is set to enable a read. However, as this is an apparatus claim, the "for a hardware debugging mode" is merely functional language which is not a structural limitation to be read into the claim. Gafken discloses a first register configured to store bits, and no structural difference in the register is needed for it to store bits which represent enable bits for a hardware debugging mode as opposed to enable bits for a read operation. (See "MPEP 2114 [R-1] Apparatus and Article Claims — Functional Language").

-A first control logic coupled to receive a plurality input signals associated with the R/L enable bits, wherein the first control logic is coupled to access the first register: (Interface 710 determines whether the R/L bit is set upon a read operation.) (Figure 7, Column 8, lines 30-32)

-And a second control logic coupled to the first register, wherein the second control logic is configured to store one or more default values in the first register in response to a reset of the processor. (Figure 7, Column 11, lines 38-55, the reset detector outputs a signal to assert all the read lock bits (HDT enable bits))

7.   Gafken teaches wherein R/L enable bits can allow or prevent read and write access to locations in memory. This prevents critical code information, such as BIOS or other start-up code, from being altered or corrupted except for in desired

instances. The desired instances include upgrading and fixing bugs. (Background, col. 1-2 and col. 14, lines 27-39).

8.   However, Gafken fails to teach the instance wherein the R/L enable bits allow access for the purpose of debugging. Therefore, the first register does not store enable bits *for a hardware debugging mode* or receive input signals *associated with the hardware debugging mode.*

9.   Yishay teaches wherein memory accesses are allowed or prevented to maintain data integrity just as Gafken teaches. However, Yishay also teaches wherein the memory access is enabled (the secure, locked mode is disabled) specifically in order to perform debugging, and that the manufacture *must be able* to easily disable secure mode to allow the debugging to occur. "Therefore, a method of disabling the secured mode must be easy enough to allow for debugging and testing." (Col. 1, lines 14-35)

10.   Therefore, it would have been obvious to one of ordinary skill in the art to use the R/L bits as enable bits for a hardware debugging mode and therefore, the signals received by the first circuit would be associated with the hardware debugging mode. This would allow the manufacturer to disable the secure mode for purposes of debugging and testing, which is highly desired, as taught by Yishay. (Col. 1, lines 14-35.)

11.   As per claim 2, Gafken, in view of Yishay, teaches the processor of claim 1,

-Wherein the first control logic is further configured to receive a request to enter

the hardware debugging mode: (The interface unit 710 receives all memory

operations, including memory read operations (a request to enter the hardware

debugging mode). Gafken, column 5, lines 60 to column 6, line 3 and column 8,

lines 21-44)

-Wherein the first control logic is further configured to read selected entries of the

one or more enable bits stored in the first register in response to the request to

enter the hardware debugging mode: (Gafken, column 7, lines 47-54, and

column 8, lines 21-44).

-And wherein the first control logic is further configured to grant or deny the

request to enter the hardware debugging mode based on the selected entries of

the one or more enable bits: (Gafken, column 7, lines 47-54, and column 8, lines

21-44).

12.   As per claim 5, Gafken, in view of Yishay, teaches the processor of claim 1,

wherein the second control logic is further coupled to receive a signal (signals

labeled, "From Bus" in figure 7) indicative of the one or more default values for the

one or more enable bits and to write the one or more default values for the one or

more enable bits into the first register in response to the reset of the processor.

(Gafken teaches wherein the R/L bits (enable bits) are loaded with default values

after a reset that is detected by the Reset Detector, which receives signals that

indicate a reset. Therefore, the Reset Detector receives a signal indicative of the

default values for the enable bits. (Gafken, column 5, lines 47-59, column 8, lines

21-44 and column 10, line 62 to column 11, lines 3-55)).

13.   As per claim 6, Gafken, in view of Yishay, teaches the processor of claim 1,

wherein the second control logic is coupled to receive a RESET signal in response

to the reset of the processor. (Gafken, figure 7, column 5, lines 47-59, column 8,

lines 21-44 and column 10, line 62 to column 11, lines 3-55. Reset Detector is

coupled to receive a RESET signal)

14.   As per claim 7, Gafken, in view of Yishay, teaches the processor of claim 1,

further comprising:

-A third register configured to store one or more microcode loader enable bits:

(W/L register, figure 7, column 6, lines 20-50, column 8, lines 21-41, column 1,

lines 13-31, Gafken)

-A third control logic coupled to receive a plurality of microcode inputs, wherein

the third control logic is coupled to access the third register: (Interface 710

contains both logic to control the access to the R/L register and logic to control

the W/L (microcode loader enable) register. Since the interface 710 can access

both the R/L and W/L registers individually, and while it is unclear how much of

the control logic for the R/L control and for the W/L control is unique to each

control logic portion respectively, the interface 710 inherently has at least some

control logic for the R/L control that is separate from the control for the W/L

control. The shared logic (including inputs) to interface 710 along with the

inherent, not shown, unique W/L control logic makes up the third control logic. (Gafken, figure 7, Column 8, lines 21-44)

-And a fourth control logic coupled to the third register, wherein the fourth control logic is configured to store one or more default values in the third register in response to a reset of the processor. (Reset Detector contains both logic to store default values to the R/L register and to the W/L (microcode loader enable) register.   Since the Result Detector has connections to both the R/L and W/L registers individually (shown in figure 7), and while it is unclear how much of the Result Detector logic is unique for the R/L control and how much is unique for the W/L control, the RESET Detector inherently has at least some control logic for the R/L control that is separate from the control for the W/L control. The shared logic (including inputs) to Reset Detector along with individual physical connections to W/L register shown in figure 7 makes up the fourth control logic. (Gafken, figure 7, column 10, line 62 to column 11, line 55)

15.   As per claim 8, Gafken, in view of Yishay, teaches the processor of claim 7, wherein the third control logic (Interface 710) is further configured to receive a request to modify microcode, wherein the third control logic is further configured to read selected entries of the one or more microcode loader enable bits stored in the third register (W/L) in response to the request to modify microcode, and wherein the third control logic is further configured to grant or deny the request to modify microcode based on the selected entries of the one or more microcode loader

enable bits. (Gafken, column 6, lines 20-50, column 7, lines 47-54, column 8, lines 30-44)

16.   As per claim 9, Gafken, in view of Yishay, teaches the processor of claim 1, further comprising: a second register (L/D) coupled to the first control logic, wherein the second register is configured to store one or more enable lock bits. (Gafken, column 8, lines 21-44, column 6, lines 51-59; when in lock-down mode, the enable bit (R/L) associated with the lock-down bit, is not modifiable.)

17.   As per claim 10, Gafken, in view of Yishay, teaches the processor of claim 9,

-Wherein the first control logic (Interface 710, figure 7) is further configured to receive a request to modify the hardware debugging mode status: (Gafken, column 8, lines 42-44, column 7, lines 47-54, column 6, lines 19-59 and column 2, line 65 to column 3, line 12)

-Wherein the first control logic is further configured to read selected entries in the one or more enable lock bits stored in the second register in response to the request to modify the hardware debugging mode status: (Gafken, column 8, lines 42-44, column 7, lines 47-54, column 6, lines 19-59 and column 2, line 65 to column 3, line 12)

-And wherein the first control logic is further configured to grant or deny the request to modify the hardware debugging mode based on the selected entries in the one or more enable lock bits. (Gafken, column 8, lines 42-44, column 7, lines 47-54, column 6, lines 19-59 and column 2, line 65 to column 3, line 12)

18.   As per claim 11, Gafken, in view of Yishay, teaches the processor of claim 9,

wherein the first register and the second register are unified into a single register

configured to store two or more bits, including one or more enable bits and one or

more enable lock bits (Gafken, figure 7, the W/L and L/D registers are unified as

they are both within the Lock Bit Array 705 and also because they are both within a

Segment N containing unified R/L, W/L, and L/D bits.)

19.   As per claim 12, Gafken, in view of Yishay, teaches the processor of claim 9,

further comprising:

-A third register configured to store one or more microcode loader enable bits:

(The W/L register of figure 7 stores one or more microcode loader enable bits.

Gafken, column 6, lines 20-50, column 8, lines 21-41, column 1, lines 13-31)

-A third control logic coupled to receive a plurality of microcode inputs, wherein

the third control logic is coupled to access the third register: (Interface 710

contains both logic to control the access to the R/L register and logic to control

the W/L (microcode loader enable) register.   Since the interface 710 can access

both the R/L and W/L registers individually, and while it is unclear how much of

the control logic for the R/L control and for the W/L control is unique to each

control logic portion respectively, the interface 710 inherently has at least some

control logic for the R/L control that is separate from the control for the W/L

control. The shared logic (including inputs) to interface 710 along with the

inherent, not shown, unique W/L control logic makes up the third control logic. (Gafken, figure 7, column 8, lines 21-44)

-And a fourth control logic coupled to the third register, wherein the fourth control logic is configured to store one or more default values in the third register in response to a reset of the processor: (Reset Detector contains both logic to store default values to the R/L register and to the W/L (microcode loader enable) register. While it is unclear how much of the Result Detector logic is unique for the R/L control and how much is unique for the W/L control, the Result Detector has connections to both the R/L and W/L registers individually (shown in figure 7), and therefore RESET Detector inherently has at least some control logic for the R/L control that is separate from the control for the W/L control. The shared logic (including inputs) to Reset Detector along with individual physical connections to W/L register shown in figure 7 makes up the fourth control logic. (Gafken, figure 7, column 10, line 62 to column 11, line 55)

20.   As per claim 13, Gafken, in view of Yishay, teaches the processor of claim 12, wherein the third control logic (Interface 710) is further configured to receive a request to modify microcode, wherein the third control logic is further configured to read selected entries in the one or more microcode loader enable bits stored in the third register (W/L) in response to the request to modify microcode, and wherein the third control logic is further configured to grant or deny the request to modify microcode based on the selected entries in the one or more microcode loader

enable bits. (Gafken, column 6, lines 20-50, column 7, lines 47-54, column 8, lines 30-44)

21.   As per claim 14, Gafken, in view of Yishay, teaches the processor of claim 12, wherein the second and fourth control logics are unified. (Gafken, figure 7 shows the second and fourth control logic are unified by the Reset Detector block)

22.   As per claim 15, Gafken, in view of Yishay, teaches the processor of claim 14, wherein the first control logic, the second control logic, the third control logic, and the fourth control logic are unified. (Gafken, figure 7 shows that the first, second, third and fourth control circuit are all located on the flash memory device 700, and are therefore all unified. The first, second, third and fourth are also unified because they are connected directly by an unlabeled wire shown in figure 7.)

23.   Claims 3-4, 35, 41, 42 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gafken et al., U.S. Patent 5,826,007, herein referred to as Gafken, in view of Yishay et al., U.S. Patent 5,704,039, herein referred to as Yishay and further in view of Short, Embedded Microprocessor Systems Design.

24.   As per claim 3, Gafken, in view of Yishay, teaches the processor of claim 1, wherein the R/L bits (enable bits) are loaded upon reset after power is removed from the processor with default values, however, does not specify how the default values are written into the R/L registers by the Reset Detector 135.

25.   Short teaches wherein non-volatile memory is ideal for storing data that is

needed upon powering on (reset), since it will not lose its data when power is turned

off. (Page 35)

26.   It would have been obvious to one of ordinary skill in the art to have the default

values for the R/L (HTD enable) bits stored in non-volatile memory since Short

teaches that non-volatile memory is well-suited for this purpose because it retains its

data even when power is shut off.

27.   As per claim 4, Gafken, in view of Yishay and Short, teaches the processor of

claim 3, wherein the second control logic is further coupled to read the one or more

default values for the one or more enable bits from the one or more non-volatile

memory cells and to write the one or more default values for the one or more enable

bits into the first register in response to the reset of the processor. (Gafken, in view

of Short, teaches wherein on a reset, default values are written into the R/L register

(first register), and wherein they come from non-volatile memory locations. (Gafken,

column 5, lines 47-59, column 11, lines 38-55 and Short, page 35)

28.   Examiner notes claims 35, 41, 42 and 53 each use the phrase "wherein the one

or more various entries are selected from the group consisting of:" followed by a list

of entries (or a similar phrase). These limitations only require *one* entry of the group

to be selected, not all.

29.   As per claim 35, Gafken teaches a method of operating a processor, the method

comprising:

-Writing one or more default values as one or more various entries in one or more

registers in response to a reset of the processor, wherein the one or more various

entries are selected from the group consisting of: one or more enable bits, one or more

enable lock bits associated with the enable bits, one or more microcode loader enable

bits, and one or more microcode loader enable lock bits. (The Reset Detector stores

default values in the R/L register (enable bits), W/L register (microcode loader enable

status), and L/D register (enable lock and microcode loader enable lock). The

appropriate default values are selected and put in the appropriate registers upon a

reset. Figure 7, Column 11, lines 3-55, column 5, lines 47-59)

30.   However, Gafken does not specify how the default values are written into the

W/L registers by the Reset Detector 135.   (Figure 3, Reset Detector, Column 5,

lines 47-59, and column 10, line 62 to column 11, lines 3-55).   Therefore, Gafken

fails to teach obtaining one or more default values, wherein obtaining the one or

more default values is selected from the group consisting of: reading the one or

more default values from one or more non-volatile memory cells, and receiving the

one or more default values as a strapped value through a pull-up or pull-down

resistor;

31.   Short teaches wherein non-volatile memory is ideal for storing data that is

needed upon powering on (reset), since it will not lose its data when power is turned

off. (Page 35)

32.   It would have been obvious to one of ordinary skill in the art to have the default

values for the R/L (enable) bits, W/L (microcode loader enable) bits and L/D (and

microcode loader lock enable) bits stored in non-volatile memory (and therefore read

out/obtained and placed in the appropriate registers) since Short teaches that non-

volatile memory is well-suited for this purpose because it retains its data even when

power is shut off.

33.   Gafken, in view of Short, teaches wherein R/L enable bits can allow or prevent

read and write access to locations in memory. This prevents critical code

information, such as BIOS or other start-up code, from being altered or corrupted

except for in desired instances. The desired instances include upgrading and fixing

bugs. (Gafken, background, col. 1-2 and col. 14, lines 27-39).

34.   However, Gafken, in view of Short, fails to teach the instance wherein the R/L

enable bits allow access for the purpose of debugging. Therefore, the first register

does not store enable bits associated with a hardware debugging mode.

35.   Yishay teaches wherein memory accesses are allowed or prevented to maintain

data integrity just as Gafken teaches. However, Yishay also teaches wherein the

memory access is enabled (the secure, locked mode is disabled) specifically in order

to perform debugging, and that the manufacture must be able for this purpose.

"Therefore, a method of disabling the secured mode must be easy enough to allow

for debugging and testing." (Col. 1, lines 14-35)

36.   Therefore, it would have been obvious to one of ordinary skill in the art to use the

R/L bits as enable bits associated with a hardware debugging mode and therefore,

the signals received by the first circuit would be associated with the hardware

debugging mode. This would allow the manufacturer to disable the secure mode for

purposes of debugging and testing, which is highly desired, as taught by Yishay.

(Col. 1, lines 14-35.)

37.   Given the similarities between claim 35 and claim 53, the arguments as stated for

the rejection of claim 35 also apply to claim 53.

38.   As per claim 41, Gafken teaches a processor, comprising:

-Means for storing one or more default values, wherein the default values are

selected from the group consisting of: enable status, enable lock status associated with

the enable status, microcode loader enable status, and microcode loader enable lock

status: (The Reset Detector stores default values in the R/L register (enable status),

W/L register (microcode loader enable status), and L/D register (enable lock and

microcode loader enable lock). The appropriate default values are selected and put in

the appropriate registers upon a reset. Figure 7, Column 11, lines 3-55, column 5, lines

47-59)

-And means for writing the one or more default values as one or more various

entries in the means for storing the one or more default values in response to a reset of

the processor, wherein the one or more various entries are selected from the group

consisting of: one or more enable bits, one or more enable lock bits associated with the

enable bits, one or more microcode loader enable bits, and one or more microcode

loader enable lock bits: (The Reset Detector stores default values in the R/L register

(enable status), W/L register (microcode loader enable status), and L/D register (enable

lock and microcode loader enable lock). The appropriate default values are selected

and put in the appropriate registers upon a reset. Figure 7, Column 11, lines 3-55,

column 5, lines 47-59)

39.   However, Gafken does not specify how the default values are written into the

WL registers by the Reset Detector 135. (Figure 3, Reset Detector, Column 5,

lines 47-59, and column 10, line 62 to column 11, lines 3-55). Therefore, Gafken

fails to teach means for obtaining the one or more default values, wherein obtaining

the one or more default values is selected from the group consisting of:

-Reading the one or more default values from non-volatile memory,

-And receiving the one or more default values as a strapped value through a pull-up

or pull-down resistor;

40.   Short teaches wherein non-volatile memory is ideal for storing data that is

needed upon powering on (reset), since it will not lose its data when power is turned

off. (Page 35)

41.   It would have been obvious to one of ordinary skill in the art to have the default

values for the R/L (enable) bits, W/L (microcode loader enable) bits and L/D (and

microcode loader lock enable) bits stored in non-volatile memory since Short

teaches that non-volatile memory is well-suited for this purpose because it retains its

data even when power is shut off.

42.   Gafken, in view of Short, teaches wherein R/L enable bits can allow or prevent

read and write access to locations in memory. This prevents critical code

information, such as BIOS or other start-up code, from being altered or corrupted

except for in desired instances. The desired instances include upgrading and fixing

bugs. (Gafken, background, col. 1-2 and col. 14, lines 27-39).

43.   However, Gafken, in view of Short, fails to teach the instance wherein the R/L

enable bits allow access for the purpose of debugging. Therefore, the first register

does not store enable bits associated with a hardware debugging mode.

44.   Yishay teaches wherein memory accesses are allowed or prevented to maintain

data integrity just as Gafken teaches. However, Yishay also teaches wherein the

memory access is enabled (the secure, locked mode is disabled) specifically in order

to perform debugging, and that the manufacture must be able for this purpose.

"Therefore, a method of disabling the secured mode must be easy enough to allow

for debugging and testing." (Col. 1, lines 14-35)

45.   Therefore, it would have been obvious to one of ordinary skill in the art to use the

R/L bits as enable bits for a hardware debugging mode and therefore, the signals

received by the first circuit would be associated with the hardware debugging mode.

This would allow the manufacturer to disable the secure mode for purposes of

debugging and testing, which is highly desired, as taught by Yishay. (Col. 1, lines

14-35.)

46.   As per claim 42, Gafken teaches a computer system, comprising: a processor,

comprising:

-Means for storing one or more default values, wherein the default values are

selected from the group consisting of: enable status, enable lock status associated with

the enable status, microcode loader enable status, and microcode loader enable lock

status: (The Reset Detector stores default values in the R/L register (enable status),

W/L register (microcode loader enable status), and L/D register (HDT enable lock and

microcode loader enable lock). The appropriate default values are selected and put in

the appropriate registers upon a reset. Figure 7, Column 11, lines 3-55, column 5, lines

47-59)

-And means for writing the one or more default values as one or more various

entries in the means for storing the one or more default values in response to a reset of

the processor, wherein the one or more various entries are selected from the group

consisting of: one or more HDT enable bits, one or more HDT enable lock bits, one or

more microcode loader enable bits, and one or more microcode loader enable lock bits:

(The Reset Detector stores default values in the R/L register (HDT enable status), W/L

register (microcode loader enable status), and L/D register (HDT enable lock and

microcode loader enable lock). The appropriate default values are selected and put in

the appropriate registers upon a reset. Figure 7, Column 11, lines 3-55, column 5, lines

47-59)

-A bridge coupled to the processor: (Figures 1 and 2 show the system of Gafken has

multiple hardware devices connected through multiple buses. A bridge is defined as, "A

hardware adapter that forwards transactions between buses." (The Authoritative

Dictionary of IEEE Standards Terms, 7th ed.) Data transactions do occur between

multiple devices on the bus, and there is inherently hardware to do so, therefore there is

inherently a bridge present to forward transactions between buses. (Column 3, lines

38-65)

-And a memory operable coupled to the processor, wherein the memory is

configured to store BIOS code: (Figure 5, column 12, lines 19 to column 14, line 26)

47.   However, Gafken does not specify how the default values are written into the

W/L registers by the Reset Detector 135. (Figure 3, Reset Detector, Column 5,

lines 47-59, and column 10, line 62 to column 11, lines 3-55). Therefore, Gafken

fails to teach means for obtaining the one or more default values, wherein obtaining

the one or more default values is selected from the group consisting of:

-Reading the one or more default values from non-volatile memory,

-And receiving the one or more default values as a strapped value through a pull-up

or pull-down resistor;

48.   Short teaches wherein non-volatile memory is ideal for storing data that is

needed upon powering on (reset), since it will not lose its data when power is turned

off. (Page 35)

49.   It would have been obvious to one of ordinary skill in the art to have the default

values for the R/L (HDT enable) bits, W/L (microcode loader enable) bits and L/D

(HDT and microcode loader lock enable) bits stored in non-volatile memory (and

therefore read out and placed in the appropriate registers) since Short teaches that

non-volatile memory is well-suited for this purpose because it retains its data even

when power is shut off.

50.   Gafken, in view of Short, teaches wherein R/L enable bits can allow or prevent

read and write access to locations in memory. This prevents critical code

information, such as BIOS or other start-up code, from being altered or corrupted

except for in desired instances. The desired instances include upgrading and fixing

bugs. (Background, col. 1-2 and col. 14, lines 27-39).

51.   However, Gafken, in view of Short, fails to teach the instance wherein the R/L

enable bits allow access for the purpose of debugging. Therefore, the first register

does not store enable bits associated with a hardware debugging mode.

52.   Yishay teaches wherein memory accesses are allowed or prevented to maintain

data integrity just as Gafken teaches. However, Yishay also teaches wherein the

memory access is enabled (the secure, locked mode is disabled) specifically in order

to perform debugging, and that the manufacture must be able for this purpose.

"Therefore, a method of disabling the secured mode must be easy enough to allow

for debugging and testing." (Col. 1, lines 14-35)

53.   Therefore, it would have been obvious to one of ordinary skill in the art to use the

R/L bits as enable bits for a hardware debugging mode and therefore, the signals

received by the first circuit would be associated with the hardware debugging mode. This would allow the manufacturer to disable the secure mode for purposes of debugging and testing, which is highly desired, as taught by Yishay. (Col. 1, lines 14-35.)

Response to Arguments

54.   Applicants arguments filed on 12/16/05 have been fully considered but are found moot in view of the new rejections above, which were necessitated by the amended portions of the claims.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not
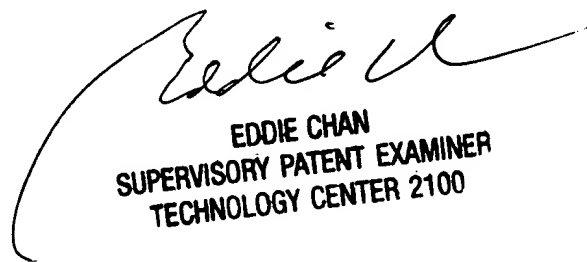
mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Kevin P Rizzuto whose telephone number is (571) 272-

4174. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for

the organization where this application or proceeding is assigned is 703-872-9306.

KPR

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